AMENDMENT TO THE CLAIMS

Claim 1 (original): A method of preventing charge buildup during fabrication of a semiconductor device, the method comprising:

coupling a first transistor to a first metal wire on a first metal level of a semiconductor device, the first transistor being configured to protect a gate of a second transistor from charge buildup, a gate of the first transistor being left floating;

forming a second metal wire in the device; and

switching ON the first transistor to discharge charges accumulated on the first metal wire during formation of the second metal wire.

Claim 2 (original): The method of claim 1 further comprising:

coupling the gate of the first transistor to ground on a topmost metal level of the device.

Claim 3 (original): The method of claim 1 wherein the second metal wire is on a second metal level of the device, the second metal level being over the first metal level.

Claim 4 (original): The method of claim 1 wherein coupling the first transistor to the first metal wire comprises:

connecting a drain of the first transistor to the first metal wire;

connecting a source of the first transistor to ground; and

connecting the gate of the first transistor to the metal wire by way of a coupling capacitor.

Claim 5 (original): The method of claim 4 wherein a value of the coupling capacitor is selected by design to switch ON the first transistor at a predetermined gate voltage.

Claim 6 (original): The method of claim 1 wherein the second metal wire is formed by physical vapor deposition.

Claim 7 (original): The method of claim 1 wherein the second transistor comprises an MOS transistor.

Claim 8 (original): The method of claim 1 further comprising:

forming a second metal level over the first metal level;

forming a third metal level over the second metal level; and

coupling the gate of the first transistor to a third metal wire on the third metal level by way of a plurality of vertically stacked vias.

Claim 9 (original): The method of claim 8 wherein the third metal wire is connected to ground.

Claim 10 (original): The method of claim 2 wherein the topmost metal level is a second metal level over the first metal level.

Claim 11 (original): The method of claim 1 wherein the first transistor comprises an nfet.

Claim 12 (cancelled)

Claim 13 (cancelled)

Claim 14 (cancelled)

Claim 15 (cancelled)

Claim 16 (cancelled)

Claim 17 (cancelled)

Claim 18 (original): A method of protecting an integrated circuit gate during a metallization process, the method comprising:

switching ON a first transistor to discharge charges accumulated on an interconnect line during a metallization process to protect a gate of a second transistor coupled to the interconnect line, a gate of the first transistor being left floating during the metallization process.

Claim 19 (original): The method of claim 18 further comprising:

coupling the gate of the first transistor to ground after the metallization process.

Claim 20 (original): The method of claim 18 wherein the metallization process comprises physical vapor deposition.